

Amendments to the Specification:

1. On page 14, please replace the original abstract filed on 05/10/2001 with the following new abstract:

ABSTRACT

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A dynamic random access memory (DRAM) is formed on a semiconductor wafer, ~~the semiconductor wafer~~ including a substrate, a thin film layer positioned on the substrate, and a photoresist layer positioned on the thin film layer. ~~Two exposure processes are employed.~~  
10 ~~The~~ A first exposure process is performed to form[[s]] first exposure regions ~~that are linear and including a plurality of lines parallel~~ to each other and covering each storage node on the photoresist layer. ~~[[The]]~~ A second exposure process is performed to form[[s]] second exposure regions that are rectangles interlaced with and  
15 perpendicular to each other on the photoresist layer and do not overlap the first exposure regions. ~~Performing a development process to the wafer removes the~~ The first exposure regions and the second exposure regions of the photoresist layer are then removed for forming to form an array photoresist layer on the thin film layer. ~~The array photoresist~~  
20 ~~layer functions~~ functioning as a mask to perform an etching process to the thin film layer for forming an array thin film layer, ~~the array thin film layer acting as~~ [[a]] storage nodes in the DRAM.

2. Please replace paragraph [0010] of the specification with the  
25 following amended paragraph:

Please refer to Fig.5 to Fig.9 of diagrams of a photolithographic process according another prior art. The photolithographic process is used to define storage nodes of a DRAM on a semiconductor wafer 40. The semiconductor wafer 40 comprises a substrate 42, a dielectric

layer 43 formed of silicon oxide, a plurality of node contacts 44 formed of doped polysilicon in the dielectric layer 43, an amorphous silicon layer 45 positioned on a surface of the dielectric layer 43 and covering each node contact 44, and a photoresist layer 47 covering a surface of the semiconductor wafer 40. The amorphous silicon layer 45 is used to form storage nodes of the DRAM.

3. Please replace paragraph [0015] of the specification with the following amended paragraph:

10 In a preferred embodiment, the present invention provides a method of forming storage nodes in a dynamic random access memory (DRAM) on a semiconductor wafer to define the position and the size of the storage nodes by ~~performed~~ performing two exposure processes. The semiconductor wafer comprises a substrate, a thin film layer positioned on the substrate, and a photoresist layer positioned on the thin film layer. The method comprises two exposure processes. The first exposure process is performed to form first exposure regions that are linear and parallel with each other on the photoresist layer. The second exposure process is performed to form second exposure regions that are interlaced with and perpendicular to each other on the photoresist layer. Performing a development process on the first exposure regions and the second exposure regions of the photoresist layer to remove[[s]] the first exposure regions and the second exposure regions of the photoresist layer, and to form an array photoresist layer on the thin film layer. The array photoresist layer is used as a mask to perform an etching process to remove portions of the thin film layer not covered by the array photoresist layer so as to form an array thin film layer, the array thin film layer being used as the storage nodes in the DRAM.

4. Please replace paragraph [0032] of the specification with the following amended paragraph:

Please refer to Fig.10 to Fig.14 of diagrams of a photolithographic process according to the present invention. The photolithographic process is used to define storage nodes of a DRAM on a semiconductor wafer 60. As shown in Fig.10, the semiconductor wafer 60 comprises a silicon substrate 62, a dielectric layer 63 formed of silicon oxide on the surface of silicon substrate 62, a plurality of node contacts 64 formed of doped polysilicon in the dielectric layer 63, an amorphous silicon layer 65 positioned on the surface of the dielectric layer 63 and covering the each node contact 64, and a photoresist layer 67 positioned on the surface the semiconductor wafer 60. The amorphous silicon layer 65 is used to form storage nodes, and each of the node contacts 64 is used to electrically connect to a drain of a MOS transistor and subsequently formed storage nodes 70.

5. Please replace paragraph [0035] of the specification with the following amended paragraph:

~~The mask~~ The mask 71 comprises a transparent substrate 72 formed of glass or quartz, and a mask pattern 73 formed of chromium film on the surface of the transparent substrate 72. The mask pattern 73 comprises a plurality of non-intersecting opaque bands 74. The bands 74 are parallel to each other, and each of the bands 74 covers an area that corresponds to the positions of a plurality of photoresist patterns 69 on the semiconductor wafer 60. The mask 75 comprises a transparent substrate 76 formed of glass or quartz, and a mask pattern 77 formed of chromium film on the surface of the transparent substrate 76. The mask pattern 77 comprises a plurality of rectangles interlaced with and perpendicular to each other formed on the chromium film and each

rectangle corners positioned on the storage nodes 70. It means that the opaque areas of the mask pattern 77 cover the areas that correspond to the positions of a plurality of photoresist patterns 69. The present invention uses the mask 71 to form a plurality of lines parallel to each other and covering each storage node 70 followed by an exposure process using the mask ~~pattern~~ 75 to cut the lines covering the storage nodes 70 to form a plurality of the array photoresist patterns 69.

6. Please replace paragraph [0036] of the specification with the following amended paragraph:

During the exposure process, a light beam penetrates through the transparent areas 80 on the mask 75 to the photoresist layer 67. Optical proximity effects cause an underexposure on areas of the photoresist pattern 69 that correspond to the corners of a transparent area 80. The formed photoresist patterns 69 possess slightly enlarged corners due to underexposure, and so the size of the formed photoresist patterns 69 is also slightly larger than that of the design patterns. These slightly larger photoresist patterns 69 not only compensate for losses in the amorphous layer 65 during the etching process, but they also compensate for the reduction in size of the storage node 70 in the subsequent resin process. Consequently, the size of the resulting formed storage node 70 is approximately the same as the design pattern.